REMARKS

Claims 1, 8, 12, 17, 20, 23, 30, 32, 33, 36, 38, 39 and 42 have been amended. The application contains claims 1-10, 12-14, 17, 19-23, 30, 32-36 and 38-42. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 8-10 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The rejection is respectfully traversed. Claim 8 has been amended to address the concerns raised in the Office Action. Accordingly, claims 8-10 are in compliance with 35 U.S.C. §112. Applicant respectfully submits that the rejection should be withdrawn and claims 8-10 allowed.

Claims 1-7, 8-10, 12-14, 23 and 42 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ichiriu in view of Chadwick. The rejection is respectfully traversed.

Claim 1 recites a method for testing a memory device. The method comprises "confirming proper operation of a control line used to enable output from a match line under test; [and] enabling output from the match line under test." The method also includes the steps of "decoding an address of a selected memory storage location corresponding to said match line under test; loading said selected memory storage location and a comparand register with a known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; outputting a result of said search operation; [and] comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test." The method further comprises "confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search

operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." Applicant respectfully submits that the cited combination fails to teach or suggest the claim 1 invention.

Specifically, as argued previously, Ichiriu merely discloses testing for parity errors of CAM cells and error correction when errors are found. There is no disclosure anywhere in Ichiriu for testing physical match lines for errors. That is, Ichiriu never has a "match line under test" because Ichiriu is only concerned with performing "simultaneous write and compare" functions and performing parity testing and error correction on the CAM cells themselves. There is no testing of match lines in Ichiriu. Likewise, there is no teaching of "confirming proper operation of a control line used to enable output from a match line under test" in Ichiriu either.

Absent these teachings, Ichiriu must fail to disclose, teach or suggest the acts of (or circuitry for) "confirming proper operation of a control line used to enable output from a match line under test; enabling output from the match line under test; decoding an address of a selected memory storage location corresponding to said match line under test; loading said selected memory storage location and a comparand register with a known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." These steps are simply not found in Ichiriu.

The Office Action acknowledges that Ichiriu fails to disclose the physical testing of match lines. To overcome this deficiency, the Office Action combines Ichiriu with Chadwick. Applicant, however, respectfully submits that Chadwick fails to disclose some of the same limitations that are missing from Ichiriu. For example, Chadwick also fails to disclose, teach or suggest "confirming proper operation of a control line used to enable output from a match line under test." Moreover, Applicant respectfully submits that Although Chadwick teaches testing match lines and making their signals accessible, Chadwick does not disclose "comparing said result of said search operation with an expected result of said search operation, [where] said expected result comprising an expected match indication on the match line under test." These features are simply not found in Chadwick.

Accordingly, claim 1 is allowable over the cited combination. Claims 2-7 depend from claim 1 and are allowable along with claim 1.

Claim 8 recites "confirming proper operation of a control line used to enable output from said match line of a set of memory cells being tested; enabling said match line of the set of memory cells being tested and disabling match lines of other sets of memory cells; storing items of data matching the data item stored in the comparand register in the set of memory cells being tested; and receiving an output signal from said match line and determining whether said output signal indicates that said set of memory cells being tested has items of stored data that match the data item stored in a comparand register." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 8 is allowable over the cited combination. Claims 9 and 10 depend from claim 8 and are allowable along with claim 8.

Claim 12 recites "a circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit

determining a status of the match line under test based on a result of a search operation and a signal on the match line under test after confirming proper operation of a control line used to generate a signal on the word line." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 12 is allowable over the cited combination. Claims 13 and 14 depend from claim 12 and are allowable along with claim 12.

Claim 23 recites a "circuit coupled to said match line under test, said corresponding word line, and a test mode match line reset signal, said circuit determining a status of a write enable signal used to generate a signal on the word line and determining a status of the match line under test based on a result of a search operation and a signal on the match line under test." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 23 is allowable over the cited combination.

Claim 42 recites "confirming proper operation of a control line used to enable output from said match line under test; enabling said match line under test; . . . loading said selected memory storage location with a known data pattern; loading a comparand register with said known data pattern; performing a search operation, for the known data pattern in the comparand register, on said memory device; and outputting a result of said search operation; comparing said result of said search operation with an expected result of said search operation, said expected result comprising an expected match indication on the match line under test; confirming proper operation of said memory device if said result of said search operation is equal to said expected result of said search operation; and indicating an error of said memory device if said result of said search operation is not equal to said expected result of said search operation." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 42 is allowable.

Moreover, it would not have been obvious to one of ordinary skill in the art to combine the cited references to achieve the claimed invention. Chadwick fails to teach or suggest how to modify Ichiriu to obtain the claimed invention. There is therefore no *prima facie* case of obviousness. Obviousness is based on factual findings. "Whether a patent claim is obvious under section 103 depends upon the answer to several factual questions and how the factual answers meld into the legal conclusion of obviousness *vel non*." *McGinley v. Franklin Sports, Inc.*, 262 F.3d 1339, 1351 (Fed. Cir. 2001). The four underlying factual inquiries are: (1) the scope and content of the prior art; (2) the differences between the claims and the prior art; (3) the level of ordinary skill in the pertinent art; and (4) secondary considerations, if any, of non-obviousness. *Graham v. John Deere Co.*, 393 U.S. 1, 17-18 (1966).

Applicant respectfully submits that there is no motivation to combine the cited references to obtain the invention of claims 1-7, 8-10, 12-14, 23 and 42. Motivation or suggestion to combine or modify prior art references "must be clear and particular, and it must be supported by actual evidence." *Teleflex, Inc. v. Ficosa North America Corp.*, 299 F.3d 1313, 1334 (Fed. Cir. 2002). Because the "genius of invention is often a combination of known elements which in hindsight seems preordained," the Federal Circuit requires a "rigorous application of the requirement for a showing of the teaching or motivation to combine prior art references." *McGinley*, 262, F.3d at 1351. Yet there is no teaching or suggestion within any of the references that provide a motivation to combine them.

The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination. *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990). Thus, a showing of an obvious combination requires more than just an amalgam of references, each of which provides one feature of the claimed invention.

The Office Action has done no more than cite a pair of references, each of which allegedly provides only part of the claimed invention, and allege that their combination renders the invention obvious. However, without the benefit of hindsight, there would have been no motivation to combine these references and the Office Action has failed to provide proof of any such motivation. This is one more reason why claims 1-7, 8-10, 12-14, 23 and 42 are allowable over the cited combination.

Accordingly, the rejection should be withdrawn and claims 1-7, 8-10, 12-14, 23 and 42 allowed.

Claims 17, 19-22, 30, 32-36 and 38-41 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Ichiriu. The rejection is respectfully traversed.

Claim 17 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a match line to provide said match signal as an output when said set of memory cells is being tested, said enabling circuitry enabling the match line after confirming proper operation of a control line." Accordingly, for at least the reasons set forth above with respect to claim 1, Applicant respectfully submits that claim 17 is allowable over Ichiriu. Claim 19 depends from claim 17 and is allowable along with claim 17.

Claim 20 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register [and] . . . enabling circuitry enabling the match line after confirming proper operation of a control line used to generate the signal on the word

line." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 20 is allowable over Ichiriu. Claims 21 and 22 depend from claim 20 and are allowable along with claim 20.

Claim 30 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register." Accordingly, for at least the reasons set forth above, claim 30 is allowable over Ichiriu. Moreover, Applicant respectfully submits that Ichiriu fails to teach or suggest "enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." The Office Action acknowledges that this feature is missing from Ichiriu, but attempts to argue that "partial" testing may occur in Ichiriu. Applicant respectfully submits that there is simply no teaching of enabling a single match line for a match line test in Ichiriu or Chadwick for that matter. This is another reason why claim 30 is allowable over Ichiriu. Claim 32 depends from claim 30 and is allowable along with claim 30.

Claim 33 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register [and] enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 33 is allowable over Ichiriu. Claims 34 and 35 depend from claim 33 and are allowable along with claim 33.

Claim 36 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and

provides a match signal when said stored items of data match the data item stored in the comparand register; and enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 36 is allowable over Ichiriu. Claims 38, 40 and 41 depend from claim 36 and are allowable along with claim 36.

Claim 39 recites "comparison circuitry that determines whether items of data stored in said set of memory cells match a data item stored in a comparand register and provides a match signal when said stored items of data match the data item stored in the comparand register; [and] for each set of memory cells, enabling circuitry that enables a single match line to provide said match signal as an output when said set of memory cells is being tested." Accordingly, for at least the reasons set forth above, Applicant respectfully submits that claim 39 is allowable.

Applicant respectfully submits that the rejection should be withdrawn and claims 17, 19-22, 30, 32-36 and 38-41 allowed.

In view of the above amendment, Applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

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